Siliconix incorporated

3 1/2-Digit A/D Converter Set

FEATURES

- Buffered Reference Input
- MOSFET Input
- Auto-Zero System
- Auto-Polarity
- Over and Under Range Signals

BENEFITS

- High Gain Stability
- Reduced Signal Loading
- Reduced Offset and Drift Over Temperature
- Reduced External Parts Count
- Easily Interfaced

APPLICATIONS

- High Performance Digital Voltmeters
- Digital Panel Meters
- Digital Instrumentation Readouts
- µP A/D Interface Subsystem
- Auto-Zeroed Microvolt or Strain Gauge Systems

DESCRIPTION

The LD110 and LD111A form a precision 3 1/2 digit A/D converter system for use in display and microprocessor based data acquisition applications. Based on Siliconix's "Quantized Feedback" technique, intrinsic features include auto-polarity, auto-zero, and ratiometric operation. Except for a stable reference, no critical components are required to achieve rated performance. The technique used offers superior linearity, normal mode rejection, and stability due to the simultaneous integration of the unknown input and the reference voltages. Unlike other conversion techniques, the integrator output voltage never represents more than 100 counts. Thus, critical, high resolution performance is not required of either the integrator or the comparator.

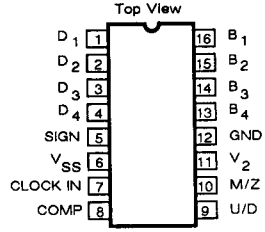
The monolithic LD111A high performance analog processor contains a bipolar comparator, a bipolar integrating amplifier, a bipolar reference amplifier, two MOSFET input unity gain amplifiers, several P-channel enhancement mode analog switches and the necessary level shifting drivers to allow the analog and digital processors to be directly interfaced. The high impedance input and reference buffer amplifiers eliminate source loading errors and provide the outstanding temperature coefficient inherent in this system. Break-before-make switch action ensures that neither the analog input nor the reference voltages will be shorted to ground at any time.

The PMOS LD110 synchronous digital processor combines the counting, storage and data multiplexing functions with the random logic necessary to control the quantized charge-balancing function of the analog processor. Seventeen static latches store the 3 1/2 digits of BCD data as well as overrange, underrange and polarity information. Nine push-pull output buffers (capable of driving one standard TTL load each) provide the sign, digit strobe and multiplexed BCD data outputs, all of which are active high. The digit scan is an interlaced format of digits 1, 3, 2, and 4.

Both devices are supplied in the 16-pin plastic DIP, and are specified for operation over the commercial, C suffix (0 to 70°C) temperature range.

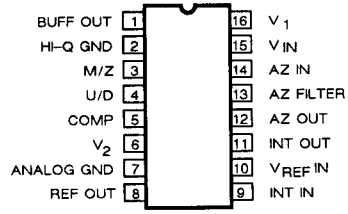
PIN CONFIGURATION

Dual-In-Line Package
Top View



Order Number: LD110CJ

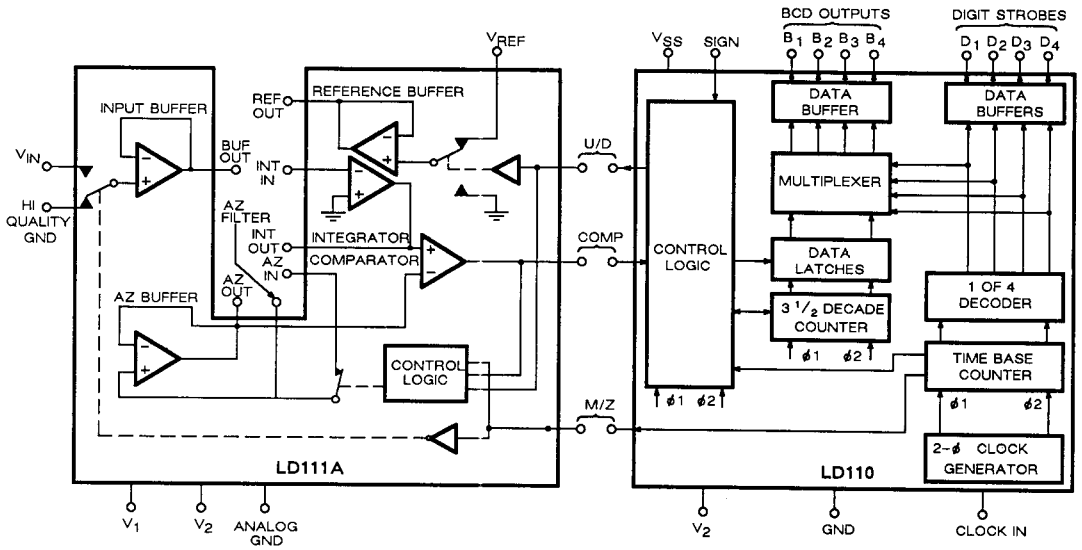
Dual-In-Line Package
Top View



Order Number: LD111ACJ

Not Recommended for New Designs

FUNCTIONAL BLOCK DIAGRAM



SWITCH STATES ARE FOR A LOGIC "0" AT U/D AND M/Z INPUTS

ABSOLUTE MAXIMUM RATINGS

I_{IN} (Pin 15, 2) ..... ±1 mA

$V_1 - V_2$ (LD111A) ..... 30 V

V_{SS} ..... 6 V

$V_{SS} - V_2$ (LD110) ..... 20 V

V On Any Pin Relative to V_{SS} (LD110) .... 0.3 V to −20 V

V_{REF} ..... V_1

Operating Temperature ..... 0 to 70°C

Storage Temperature ..... −65 to 125°C

Power Dissipation (Package)* ..... 750 mW

* Device mounted with all leads welded or soldered to PC Board. Derate 6.3 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V_1 = 12 V, V_2 = −12 V, V_{SS} = 5 V, V_{REF} = 8.2 V, R_1 = 100 kΩ	LIMITS: T_A = 25 °C TYP [d]	MIN [b]	MAX [b]	UNIT
SYSTEM						
Analog Input Range	V_{ANALOG}			−2	2	V
Linearity			0.02			% rdg
Noise		Noise apparent when going from one steady reading to another.	0.1			LSB_{p-p}

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SYSTEM (Cont'd)						
Gain T.C.			5			ppm/°C
Normal Mode Rejection	NMR	f_{NOISE} = 60 Hz	40			dB
Clock Frequency	f_{in}	50 % Duty Cycle	30.7	2	250	kHz
ON Resistance Auto Zero Switch	$r_{DS(ON)}$	$V_{AZ(IN)}$ = −4.0 V, I_S = −30 µA	6		20	kΩ
INPUT						
Clock Input Current LOW	I_{CL}	$V_{CLOCK(IN)}$ = 0.4 V		−500		µA
Input Bias Current	I_{IN}		4			pA
COMP, LD110	I_{INL}	V_{IN} = −12 V	−700	−1500	−50	µA
AMPLIFIER						
Reference Buffer	I_{SOURCE}	V_{OUT} = 0 V; $V_{INL(U/D)}$ = 0.8 V	−800		−400	µA
AZ Buffer	I_{SINK}	V_{AZ} = −4 V	800			µA
Input Buffer	I_{SINK}	V_{IN} = −2 V	800	400		µA
	I_{SOURCE}	V_{IN} = 2 V	−100		−50	µA
AZ Buffer	V_{OS}			−100	100	mV
OUTPUT						
Measure/Zero Voltage, Low	V_{OL1}	I_{OL} = 150 µA			0.6	V
Measure/Zero Voltage, High	V_{OH1}	I_{OH} = −200 µA		2.4		V
Up/Down Logic Voltage, Low	V_{OL2}	I_{OL} = 250 µA			0.6	V
Up/Down Logic Voltage, High	V_{OH2}	I_{OH} = −200 µA		2.4		V
Analog Comparator Voltage	V_{OH3}	I_{OH} = −100 µA		2.4		V

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ELECTRICAL CHARACTERISTICS [a]

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OUTPUT (Cont'd)						
Digits, Bits Voltage, Low	V_{OL3}	I_{OL} = 1.6 mA			0.6	V
Sign Voltage, Low	V_{OL4}	I_{OL} = 1.6 mA			0.65	V
Data Bits Voltage, High	V_{OH4}	I_{OH} = −200 µA		2.4		V
Digits, Sign Voltage, High	V_{OH5}	I_{OH} = −800 µA		2.4		V
SUPPLY						
V_1 Supply Current LD111A	I_1		2.2		4	mA
V_2 Supply Current LD111A	I_{2A}		−1.8	−4		mA
V_2 Supply Current LD110	I_{2D}		−17	−23		mA
V_{SS} Supply Current LD110	I_{SS}		17.4		24	mA
Power Supply Rejection Ratio, V_1	$PSRR_1$		85	80		dB
Power Supply Rejection Ratio, V_2	$PSRR_2$		65	60		dB
Reference Voltage Rejection		R_{REF} = R_2 = 100 kΩ, V_{IN} = 2 V	1			% Δ rdg per ΔV_{REF}

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

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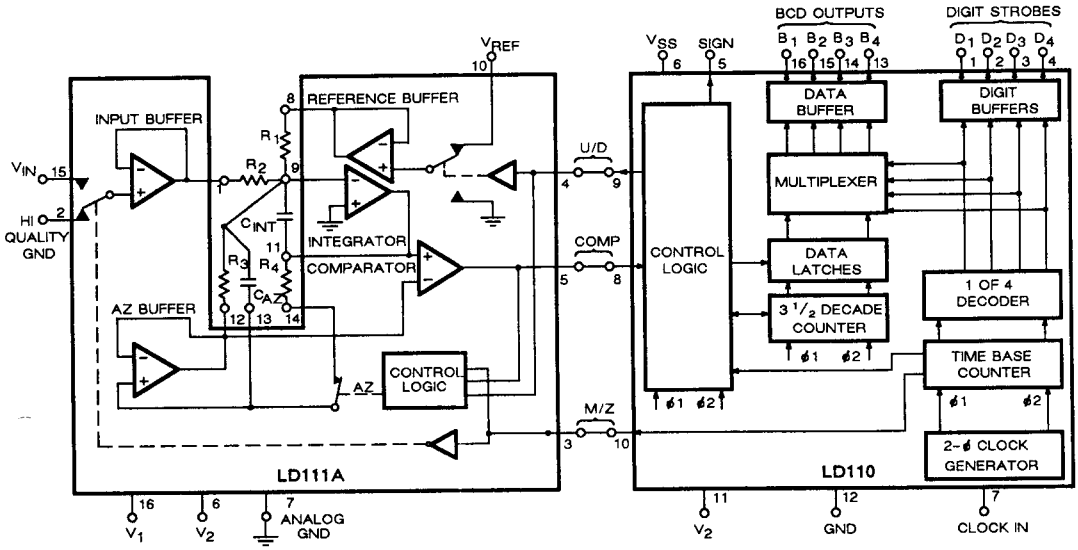
FUNCTIONAL OPERATION



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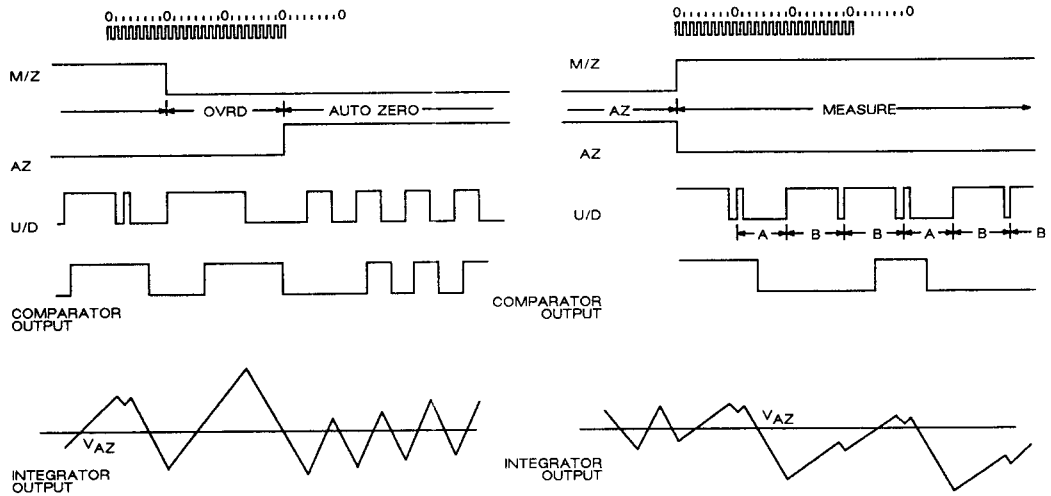

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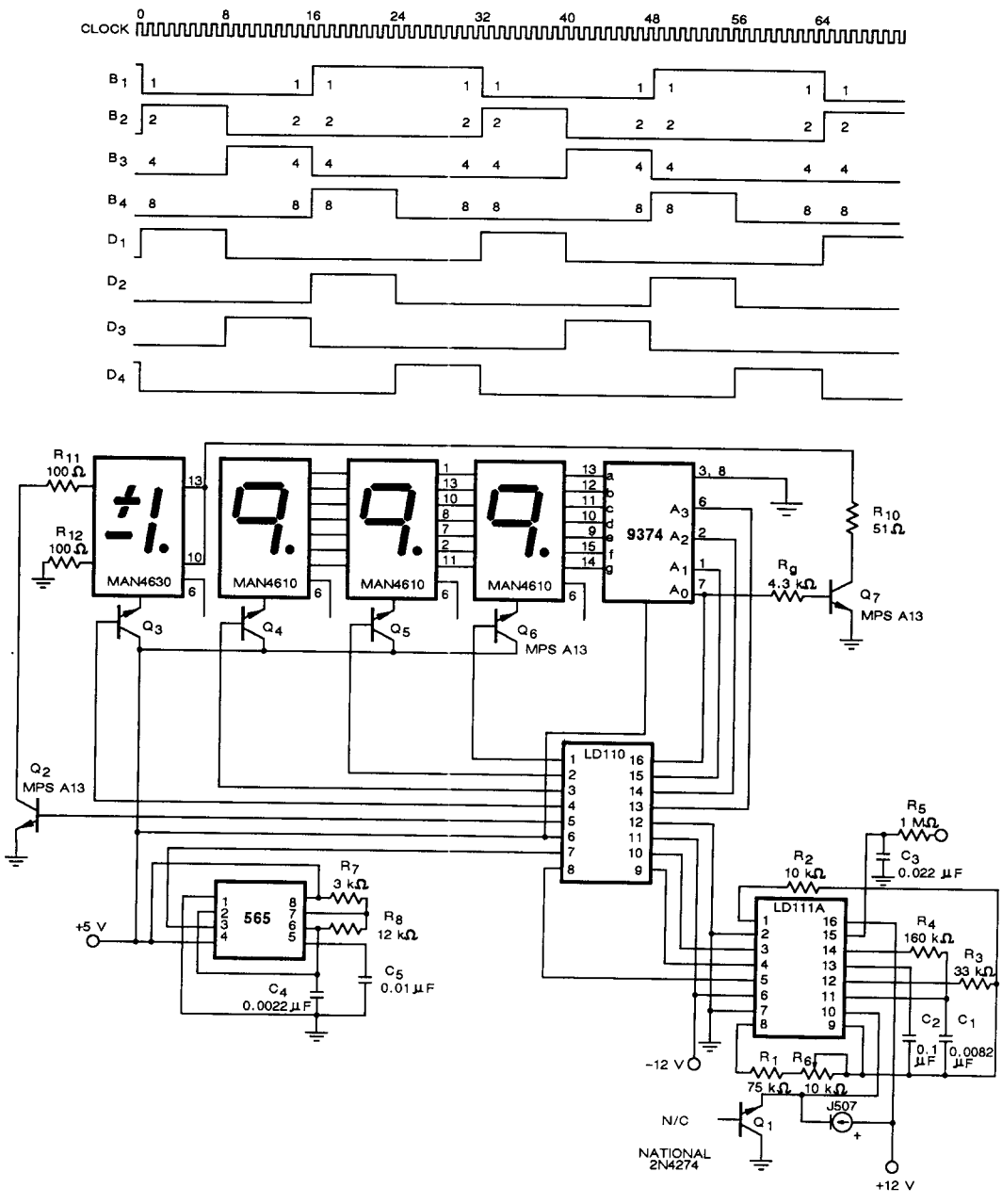
CLOCK
0
8
16
24
32
40
48
56
64
B1
B2
B3
B4
D1
D2
D3
D4
R11 100Ω
R12 100Ω
MAN4630
MAN4610
MAN4610
MAN4610
9374
R10 51Ω
Rg 4.3 kΩ
Q7 MPS A13
Q3
Q4
Q5
Q6 MPS A13
Q2 MPS A13
LD110
LD111A
R5 1 MΩ
C3 0.022 µF
R2 10 kΩ
R4 160 kΩ
R3 33 kΩ
C2 0.1 µF
C1 0.0082 µF
R1 75 kΩ
R6 10 kΩ
J507
N/C
Q1
NATIONAL 2N4274
-12 V
+12 V
+5 V
565
R7 3 kΩ
R8 12 kΩ
C4 0.0022 µF
C5 0.01 µF

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